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Fig. 20a

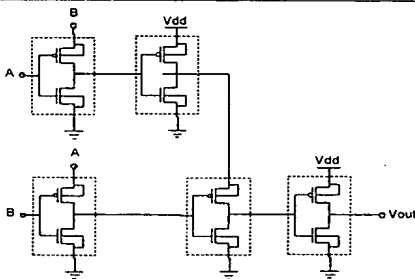
XOR

Fig. 20c

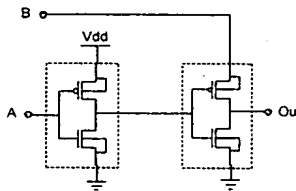
AND

Fig. 20e

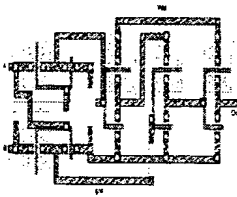
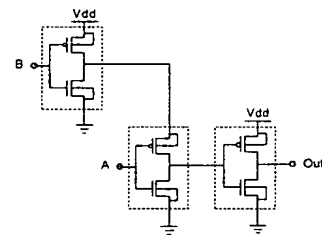
OR

Fig. 20b.

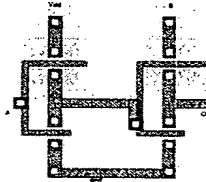


Fig. 20d

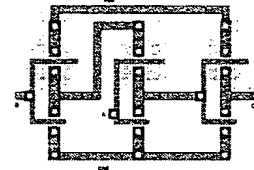


Fig. 20f

Fig. 20a

Fig. 20b

Fig. 20c

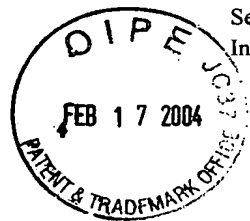
Fig. 20d

Fig. 20e

Fig. 20f

Fig. 20

Figure 20



Serial No.: 10/648,474

Inventor: MORGENSHEIN et al

ANNOTATED MARKED-UP DRAWING

Sheet: 1 of 2

Title: LOGIC CIRCUIT AND METHOD OF LOGIC CIRCUIT DESIGN

Fig 19a

Fig 19b

Fig 19c

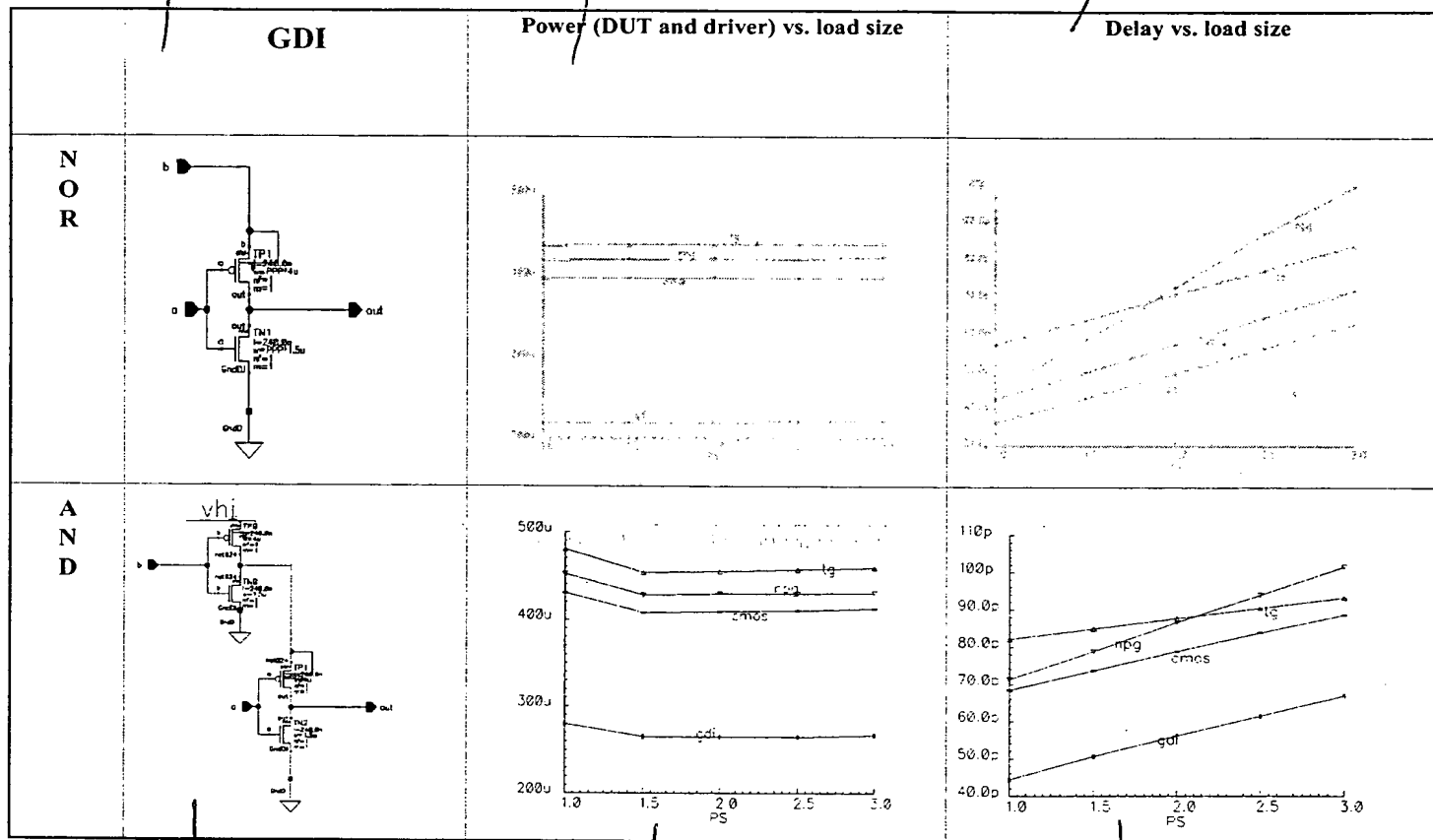


Fig 19d

Fig 19e

Fig 19f

Fig 19a
Fig 19b
Fig 19c
Fig 19d
Fig 19e
Fig 19f

Fig. 19

Figure 19